Course objective  The purpose of this course is for the students to have a practical laboratory experience in digital computing systems; to apply the concepts of basic combinational logic circuits, sequential circuit elements, and programmable logic in the laboratory setting; to develop familiarity and confidence with designing, building and testing digital circuits, including the use of CAD tools; and to develop team-building skills and enhance technical knowledge through both written assignments and design projects.

Course outline  Laboratory projects will use a PC-based CAD environment that supports schematic capture, logic simulation, and HDL-based logic synthesis on FPGAs (field-programmable gate arrays). Small-scale integrated circuits will be used for early labs, then HDL-based logic synthesis on FPGA-based design boards will be used for more advanced design implementations, including exposure to mixed design-entry methods. The semester will culminate with design projects specified and undertaken by teams of three to five students. Technical writing skills are developed through laboratory reports, project documentation, and an oral presentation.

Topics:
- CAD Tools
- Logic Synthesis using an HDL
- HDL models of basic gates and logic operations
- Combinational design using multiple methods: primitive gates, schematic capture for FPGAs, and VHDL
- HDL based simulation and synthesis with FPGAs
- Examination of real timing issues on hardware using timing simulation, oscilloscope, and logic analyzer
- State machine specification, design, and simulation
- State machine implementation with multiple methods
- Design verification with logic analyzer
- HDL models of data storage elements
- ROM and RAM implementations on FPGA boards
- Hardware design of a simple computer with ALU, registers, control unit, memory, instructions, and I/O
- HDL-based simple computer simulation and implementation on FPGA board
- Machine language and assembly language programming for the simple computer
- Simulation and implementation of programs on the FPGA board
- Final design project problem specification (examples: video game, control application, robot, or contest)
- Hardware and tools available to solve the final design project problem
- Project engineering issues: top-down vs. bottom-up design, hierarchical decomposition, and modularity

Lectures and Labs  Lecture is 1 hour long; lab is 3 hours long. There are 8 lectures and 8 labs, excepted for the in-class Exam, the remaining weeks of the semester will be dedicated to the final project.
Instructor  Stéphanie ARAVECCHIA, office 220, level 2
Email: stephanie.aravecchia@georgiatech-metz.fr

Office hours  The office hours are scheduled every Tuesday from 9:30 am to 11:30 am (or by appointment)

Courses prerequisite  ECE 2020/2030, ECE 2035/2036\textsuperscript{1} or CS 2110\textsuperscript{1}

Class Website  https://canvas.gatech.edu/
http://powersof2.gatech.edu/2031/ece2031.html
http://upcp.ece.gatech.edu/2031.html

Other Materials:
ECE 2031 Workbook (available at the main course website)
ECE 2031 Chip Set (Provided by GTL)
Protoboard (Provided by GTL)
Wire Kit (Provided by GTL)

Honor code  GT Academic Honor Code is strictly enforced at GT Lorraine. Adherence to the Georgia Tech Honor Code is expected and all suspected instances of academic misconduct will be reported to the Dean of Students. It is your responsibility to ask for clarification if collaboration guidelines, test-taking policies, etc. are not clear. You will find detailed information at http://osi.gatech.edu/content/honor-code. Students may discuss assignments in general terms with one another, but all work should be generated individually. Copying or allowing peers to copy all or portions of any assignment is considered plagiarism and is expressly forbidden.

Grading  Your grade will be determined using the following weighting.

<table>
<thead>
<tr>
<th>Component</th>
<th>Weightage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Participation</td>
<td>5%</td>
</tr>
<tr>
<td>Lab Reports</td>
<td>20%</td>
</tr>
<tr>
<td>Prelab Quizzes</td>
<td>25%</td>
</tr>
<tr>
<td>One or more Lab Practical Exercises</td>
<td>10%</td>
</tr>
<tr>
<td>Final Project</td>
<td>20%</td>
</tr>
<tr>
<td>In-class Exam</td>
<td>20%</td>
</tr>
</tbody>
</table>

There is no final Exam, an in-class Exam will be scheduled two to three weeks after Lab #8. You may give a final project presentation and/or turn in a final report during the last week of class. The written final report may be due during finals week.
In-class exam is closed books, closed notes, no computer or cell phone allowed. Practical exercises are open books and open notes.
Up to 10\% of your total grade can be lost for not keeping the lab clean. All letter grade assignments are made by the instructor. Most assignments are individual assignments. This includes pre-lab work, laboratory reports, homework assignments, computer simulations, and exams. You are expected to fully participate in all group assignments associated with the final project.
Be familiar with the course websites, especially the course overview and lab results sections in the canvas website. These describe the expectations for the assignments you will turn in. The ECE 2031 Workbook has more details about grades, assignments, late policies, grade disputes, missed quizzes, etc.

Open Lab  Hopefully you will complete all lab assignments during your allotted time. Additional open lab hours will be held as needed, typically immediately after the scheduled lab times. You may use the lab during other class sections provided there is enough equipment. However, priority always goes to students in the current section.

\textsuperscript{1}may be taken concurrently
Attendance policy  Attendance will be taken at the beginning of each class. For more information about class attendance at Georgia Tech, you may go to http://www.catalog.gatech.edu/rules/4/. It should be noted that attendance is mandatory for all laboratory sessions. Any absence from an exam or laboratory session will result in a grade of zero, which may be made up at the discretion of the instructor.

Course Outcomes  Upon successful completion of this course, students should be able to:

1. implement combinational logic circuits both with TTL devices on a protoboard and within a complex PLD.
2. analyze the timing of digital circuits with oscilloscopes and logic analyzers.
3. design and implement state machines to meet design specifications.
4. design circuits with a graphical schematic CAD editor.
5. simulate circuits within a CAD tool and compare to design specifications.
6. design, implement, and simulate circuits using VHDL.
7. implement a simple computer within a PLD.
8. write machine language programs and assembly language programs for the simple computer.
9. use a complex sequential logic circuit as part of a solution to an open-ended design problem.
10. write laboratory reports and documentation conforming to technical writing standards.
11. work effectively as team members to develop and write a group report.
12. work effectively as team members to design an approved project.

Student-Faculty Expectations Agreement  At Georgia Tech we believe that it is important to strive for an atmosphere of mutual respect, acknowledgement, and responsibility between faculty members and the student body. See http://www.catalog.gatech.edu/rules/22/ for more information.

Disabilities  Georgia Tech offers accommodation to students with disabilities, this policy is extended to GT Lorraine. If you need any accommodation, then inform your instructor and Mrs Corinne Guyot with a certificate from the Office of Disability Services.